Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION**

1. **NULL**
2. **–INPUT**
3. **+INPUT**
4. **V-**
5. **NC**
6. **OUTPUT**
7. **V+**
8. **NULL**

**.055”**

**.109”**

**8 7 6**

**1 2 3 4**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Isolated**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .055” X .109” DATE: 9/9/21**

**MFG: ANALOG DEVICES THICKNESS .012” P/N: OP27NBC**

**DG 10.1.2**

#### Rev B, 7/1